WHAT IS CLAIMED is:

1. A semiconductor device comprising:

a semiconductor substrate;

at least one electrode pad formed above the semiconductor substrate;

a multilevel interconnection configuration disposed between the electrode pad and the semiconductor substrate, the multilevel interconnection configuration including a number of interconnection layers;

a first insulating film of low dielectric constant which is formed above the semiconductor substrate to insulate the interconnection layers from one another; and

a dummy interconnection configuration formed at least within the first insulating film around the periphery of the electrode pad.

2. The semiconductor device according to claim 1, wherein the dummy interconnection configuration is formed in a position corresponding to a displacement of a wire to be bonded to the electrode pad from the periphery of the electrode pad.

3. The semiconductor device according to claim 1, wherein the distance between the dummy interconnection configuration and the multilevel interconnection configuration is set substantially equal to the minimum distance in design rules.

4. The semiconductor device according to claim 1, wherein the dummy interconnection configuration comprises interconnection layers corresponding in number to the interconnection layers of the multilevel interconnection configuration and vias which interconnect the interconnection layers.

5. The semiconductor device according to claim 1, wherein the dummy interconnection configuration is formed in the shape of a ring around the periphery of the electrode pad.

6. The semiconductor device according to claim 5, wherein the dummy interconnection configuration formed in the shape of a ring has its portion made open.

7. The semiconductor device according to claim 4, wherein the dummy interconnection configuration is composed of a plurality of interconnection patterns which are square or rectangular in plane shape and the interconnection patterns are arranged at regular intervals around the periphery of the electrode pad.

8. The semiconductor device according to claim 1, wherein the insulating film of low dielectric film is 20 GPa or less in Young's modulus.

9. The semiconductor device according to claim 7, wherein the dummy interconnection configuration is also present in a layer in which the electrode pad is formed.

10. The semiconductor device according to claim 1,

wherein the dummy interconnection configuration is formed at least within the range of thickness of the insulating film of low dielectric constant.

11. The semiconductor device according to claim 1, further comprising:

a second insulating film formed to cover the first insulating layer with the electrode pad exposed; and

a third insulating film formed on the second insulating film and having a Young's modulus of 20 GPa or less.

12. The semiconductor device according to claim 11, wherein the third insulating film has its top made water repellent.

13. A semiconductor device comprising:

a semiconductor substrate;

at least one electrode pad formed above the semiconductor substrate;

a multilevel interconnection configuration disposed between the electrode pad and the semiconductor substrate, the multilevel interconnection configuration including a number of interconnection layers;

a first insulating film of low dielectric constant which is formed above the semiconductor substrate to insulate the interconnection layers from one another;

a first dummy interconnection configuration formed at least within the first insulating film around the

periphery of the electrode pad; and

a second dummy interconnection configuration formed on the opposite side of the first dummy interconnection configuration from the electrode pad.

14. The semiconductor device according to claim 13, wherein the first dummy interconnection configuration is formed in a position corresponding to a displacement of a wire to be bonded to the electrode pad from the periphery of the electrode pad.

15. The semiconductor device according to claim 13, wherein the first dummy interconnection configuration is composed of a plurality of interconnection patterns which are square or rectangular in plane shape and the interconnection patterns are arranged at regular intervals around the periphery of the electrode pad.

16. The semiconductor device according to claim 13, wherein the second dummy interconnection configuration is formed in the shape of a ring around the periphery of the electrode pad.

17. A semiconductor device comprising:

a semiconductor substrate;

a plurality of electrode pads formed above the semiconductor substrate;

a multilevel interconnection configuration disposed between the electrode pads and the semiconductor substrate, the multilevel interconnection

configuration including a number of interconnection layers;

a first insulating film of low dielectric constant which is formed above the semiconductor substrate to insulate the interconnection layers from one another; and

a dummy interconnection configuration formed at least within the first insulating film around the periphery of the electrode pads.

18. The semiconductor device according to claim 17, wherein the dummy interconnection configuration is formed in a position corresponding to a displacement of wires to be bonded to the electrode pads from the periphery of the electrode pad.

19. The semiconductor device according to claim 17, wherein the dummy interconnection configuration is composed of a plurality of interconnection patterns which are square or rectangular in plane shape and the interconnection patterns are arranged at regular intervals around the periphery of the electrode pads.

20. The semiconductor device according to claim 17, wherein the dummy interconnection configuration is formed in the shape of a ring around the periphery of the electrode pads.